ECE 257
Linear Integrated Analog Circuits
Switched-Capacitor Circuits

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Switched Capacitor Circuits

• Basics Operation
• Functional Operation
  ▪ Switched-Capacitor Integrator
  ▪ Discrete-Time Signal Processing
  ▪ Switched Capacitor Filters
  ▪ Sample and Hold Circuits
  ▪ Gain Stages
• Non-Ideal effects and Practical Solutions
  ▪ Analysis of Sampling Switches
  ▪ Charge injection and Clock Feed-through
  ▪ Bottom-Plate Sampling
  ▪ Effect of op-amp non-idealities
  ▪ Noise
  ▪ Correlated double-sampling
Why SC Circuits?

• SC Circuits
  ▪ Discrete-time systems

• Accurate realization of filters and gains
  ▪ Accuracy related to matching of capacitors
  ▪ No need to resistors
  ▪ Performance Independent of absolute values of C

• Highly linear
  ▪ Independent of shape of waveforms
  ▪ Only settling accuracy is important
Basic Operation: SC Resistor

- $I_{\text{avg}} = \frac{C(V_1 - V_2)}{T}$
- $R_{eq} = \frac{T}{C} = \frac{1}{fC}$
- Low-frequency approximation
Basic Switched-Capacitor Integrator

- Phase Φ1: C1 is charged up to Vin (Q=C1Vin)
- Phase Φ2: C1 charge (Q=C1Vin) is transferred into C2
- Charge transfer equation:

\[
C_2 V_{o}(nT - T/2) = C_2 V_{o}(nT - T) - C_1 V_{i}(nT - T)
\]
\[
C_2 V_{o}(n) = C_2 V_{o}(n - 1) - C_1 V_{i}(n - 1)
\]
\[
H(z) = \frac{V_{o}(n)}{V_{i}(n)} = -\frac{C_1}{C_2} \frac{z^{-1}}{1 - z^{-1}}
\]
Sensitivity to Parasitic Capacitance

- Basic SC equal resistor is sensitive to parasitics

\[ Vo(n) = - \frac{C1 + C_{p1}}{C2} \frac{z^{-1}}{1 - z^{-1}} Vi(n) \]
Parasitic-Insensitive Integrator

- Non-inverting integrator
- Delayed

\[ H(z) = \frac{V_o(n)}{V_i(n)} = \frac{C_1}{C_2} \frac{z^{-1}}{1 - z^{-1}} \]

\[ C_2 V_o(n) = C_2 V_o(n-1) + C_1 V_i(n-1) \]
Parasitic-Insensitive Integrator: Operation

- $C_{p2}$: Always connected to ground
- $C_{p1}$: Connected to ground in $\Phi2$
Parasitic-Insensitive Integrator: Delay Free

- Inverting integrator
- Delay Free

\[ H(z) = \frac{V_o(n)}{V_i(n)} = -\frac{C_1}{C2} \frac{1}{1 - z^{-1}} \]  \[ C_2V_o(n) = C_2V_o(n-1) - C_1V_i(n) \]
Switched Capacitor Filters

• H(s) to H(z)
  ▪ Bilinear Transform: Accurate \[ s = -\frac{2 \left(1 - z^{-1}\right)}{T \left(1 + z^{-1}\right)} \]
  ▪ Impulse invariant: Simple but not accurate \[ h[n] = Th_c(nT) \]
Implementing H(z) by SC Circuits

\[ \frac{1}{C_A 1 - z^{-1}} \]
Example: First-Order Filter
First-Order Filter

\[ H(z) = -\left(\frac{C_1 + C_2}{C_A}\right)z + \frac{C_1}{C_A} \left(1 + \frac{C_3}{C_A}\right)z - 1 \]

- **DC Gain:** \( H(1) = -\frac{C_2}{C_3} \)
- **Pole:** \( z_p = \frac{C_A}{C_A + C_3} \)
- **Zero:** \( z_z = \frac{C_1}{C_1 + C_2} \)
Design Example

• First order filter: -3dB @ 10kHz, 0 @ 50kHz, fs=100kHz, DC Gain=1
• Zero at 50kHz: zz=-1, (Negative capacitor)
• Using bilinear transform: zp=10kHz, s=2/T(z-1)/(z+1) ⇒ zp=.53327

• $H(z): H(z) = K \frac{(z+1)}{z-0.53327}$  \hspace{1cm} H(1)=1 ⇒ K=0.23337

• Assume $C_A=10\text{pf}$ ⇒
  - $C_1=4.376\text{pF}$
  - $C_2=-8.752\text{pF}$
  - $C_3=8.752\text{pF}$

• Implementing $C_2$: Cross-couple it in a fully differential design
Switch Sharing

- Removing redundant switched
Biquad Filter: Low-Q

- Biquad: General second-order system
- Any filter can be realized by cascading biquads and first-orders
- Low-Q and High-Q implementation
Low-Q Biquad Filter: CT Implementation
Low-Q Biquad Filter: SC Implementation

From Analog Integrated Circuit Design (Johns & Martin)
Low-Q Biquad Filter: z domain flow-graph

\[ H(z) = \frac{a_2 z^2 + a_1 z + a_0}{b_2 z^2 + b_1 z + 1} \]

- \( K_3 = a_0 \)
- \( K_2 = a_2 - a_0 \)
- \( K_1 K_5 = a_0 + a_1 + a_2 \)
- \( K_6 = b_2 - 1 \)
- \( K_4 K_5 = b_1 + b_2 + 1 \)

• One degree of freedom for \( K_1, K_4 \) and \( K_5 \)
• Optimum choice for dynamic range: \( K_4 = K_5 = \sqrt{b_1 + b_2 + 1} \)
CT to SW Conversion

- Impulse invariance
- Rewrite $H(z) = -\frac{(K_2 + K_3)z^2 + (K_4K_5 - K_2 - 2K_3)z + K_3}{(1 + K_6)z^2 + (K_4K_5 - K_6 - 2)z + 1}$ to $H(z) = -\frac{K_4K_5 + K_2(z^{1/2} - z^{-1/2})z^{1/2} + K_3(z^{1/2} - z^{-1/2})^2}{K_4K_5 + K_6(z^{1/2} - z^{-1/2})z^{1/2} + (z^{1/2} - z^{-1/2})^2}$

- For $z^{-1/2}$ and $z^{1/2}$ we have:
  $$z^{1/2} = \cos\left(\frac{\omega T}{2}\right) + j\sin\left(\frac{\omega T}{2}\right)$$
  $$z^{-1/2} = \cos\left(\frac{\omega T}{2}\right) - j\sin\left(\frac{\omega T}{2}\right)$$

  - $H(j\omega)$ is:
    $$H(z) = -\frac{K_1K_5 + jK_2\sin(\omega T) + (4K_3 + 2K_2)\sin^2\left(\frac{\omega T}{2}\right)}{K_4K_5 + jK_6\sin(\omega T) + (4 + 2K_6)\sin^2\left(\frac{\omega T}{2}\right)}$$

  - For $\omega T \ll 1$
    $$H(z) = -\frac{K_1K_5 + jK_2(\omega T) + (K_3 + K_2/2)(\omega T)^2}{K_4K_5 + jK_6(\omega T) + (1 + K_6/2)(\omega T)^2}$$

  - $K_4 = K_5 = \omega_0 T$, $K_6 = \omega_0 T/Q$
- For high Q, large capacitor ratio required
Biquad Filter: High-Q

- Biquad HQ

\[ H(z) = \frac{-K_3z^2 + (K_1K_5 + K_2K_5 - 2K_3)z + K_3 - K_2K_5}{z^2 + (K_4K_5 + K_5K_6 - 2)z + (1 - K_5K_6)} \]
Sample and Hold Circuits: Flip-Around

- Fast: OTA out does not change: Relaxed SR
- Feedback factor = 1
- Common-Mode Issue: Input signal CM should be equal to OTA CM
Flip-Around S&H: Fully Differential
Sample and Hold Circuits: Two-Capacitor

- OTA Settles: Slower
- Insensitive to CM difference
Gain Stage I

- Same as S&H: $G = -\frac{C_1}{C_2}$
Gain Stage II

- $G = 1 + \frac{C_1}{C_2}$
Practical Issues and Non-Idealities

- MOS Sampling
- Speed
- Linearity
- Switch bootstrapping
- Charge Injection
- Jitter
- Noise
MOS T&H: Simulation
MOS S&H: Tracking Speed & Distortion

- Simple RC model: \( V_o = V_i \left( 1 - e^{\frac{-t}{\tau}} \right) \)

- \( \tau = \frac{1}{RC} \)

- \( R \approx \frac{1}{\mu L \frac{W}{L} (V_{DD} - V_I - V_I)} \)

- R is non-linear!

- \( V_o = V_i \left( 1 - e^{\frac{-t}{2\tau \left( \frac{V_i}{V_{DD} - V_T} \right)}} \right) \)

- Tracked signal has harmonic distortion!
MOS S&H: Tracking Distortion

- $W=10$, $L=0.18$, $C_{in}=1pF$, $f_s=50M$, $f_{in}=1.56M$, $V_{in}=0.5V$, 

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Improving Tracking Speed: T-GATE

- Not a good choice for low-voltage technologies
Improving Tracking Speed: Bootstrapping

- Improving R by increasing $V_{GS}$
- No terminal-to-terminal voltage exceeds $V_{DD}$
- Overdrive Independent of $V_i$
Improving Tracking Speed: Bootstrapping

* test bench for switch

Voltages (ln)

Time (ln) (TIME)

0 50n 100n 150n 200n 250n 300n 350n
Charge Injection and Clock Feed-through

- Error in sampled voltage due to charge injection and clock feed-through
- Clock feed-through
  - Independent of $V_i$
  \[
  \Delta V_o = \frac{C_{gd}}{C_{gd} + C_L} V_{DD}
  \]
- Charge injection
  - Depends on $V_i$
  - Body effect
  \[
  \Delta V_o = \beta \frac{WLC_{ox}(V_{DD} - V_i - V_T)}{C_L}
  \]
- Charge injection causes harmonic distortion
Canceling Charge Injection

• Dummy transistor
  ▪ Dummy transistor: half size

• Tgate as switch
  ▪ NMOS and PMOS have same size
Canceling Charge Injection: Fully Differential
Bottom-Plate Sampling

- Q2 turns off first $\Rightarrow$ Q2 induces *Constant* charge in C1
- Q1 turns off later $\Rightarrow$ Q1 does not add charge in C1
- Induced error is independent of Vin
SC Circuits with Bottom-Plate Sampling
Clock Jitter

- Jitter ($\Delta t$): Uncertainty in rising and falling of clock signal
  - $\Delta t$ in the range of 1-100ps
  - $\Delta t \Rightarrow \Delta v$ in sampling
Correlated Double Sampling

- Canceling opamp offset and 1/f noise
- Store offset in C2’ during sampling phase
Effect of Op-Amp

- Limited Gain
- Limited Settling
  - Linear settling
  - Nonlinear settling
- Non-Linearity
  - Variable gain
  - Slewing
  - Switched
- Noise
Limited Gain of op-amp

\[ H(z) = \frac{V_o(n)}{V_i(n)} = \frac{C_1}{C_2} \left(1 - \frac{1}{1 - \frac{C_1}{A C_2}}\right) \left(1 - \varepsilon z^{-1}\right) \]

\[ 1 - \varepsilon = \frac{1}{1 + \frac{A}{C_1}} \]

\[ \lambda = \frac{1}{A} \left(1 + \frac{C_1}{C_2}\right) \]

\[ \text{Gain} = \frac{C_1}{C_2} \left(1 + \frac{1}{A} \frac{C_1 + C_2}{C_2}\right) \]

- SC Integrator: Convert to low-pass filter
- Sample and hold: Gain error
Linear & Nonlinear Settling

- Linear Settling: Caused gain error
- Nonlinear Settling: Input-dependent response → harmonic distortion
  - High-Slew-Rate op-amp required!

\[
H(z) = \frac{V_o(n)}{V_i(n)} = \frac{C_1}{C_2} \left(1 - e^{-\frac{T}{\tau}} \right) \frac{z^{-1}}{1 - z^{-1}}
\]
Linear Settling: Feedback Factor

- Larger gain $\Rightarrow$ Larger $C_1/C_2$ $\Rightarrow$ Slower settling
- Large input parasitic $C_P$ $\Rightarrow$ Slow settling

\[ \tau = \frac{1}{2\pi f_T} \frac{C_1 + C_2 + C_P}{C_2} \]
Op-Amp Noise

- Noise:
- KT/C Noise
- Op-Amp noise