

Reducing Round-off Error in An ADSL Modem with Block- Floating-Point Structure

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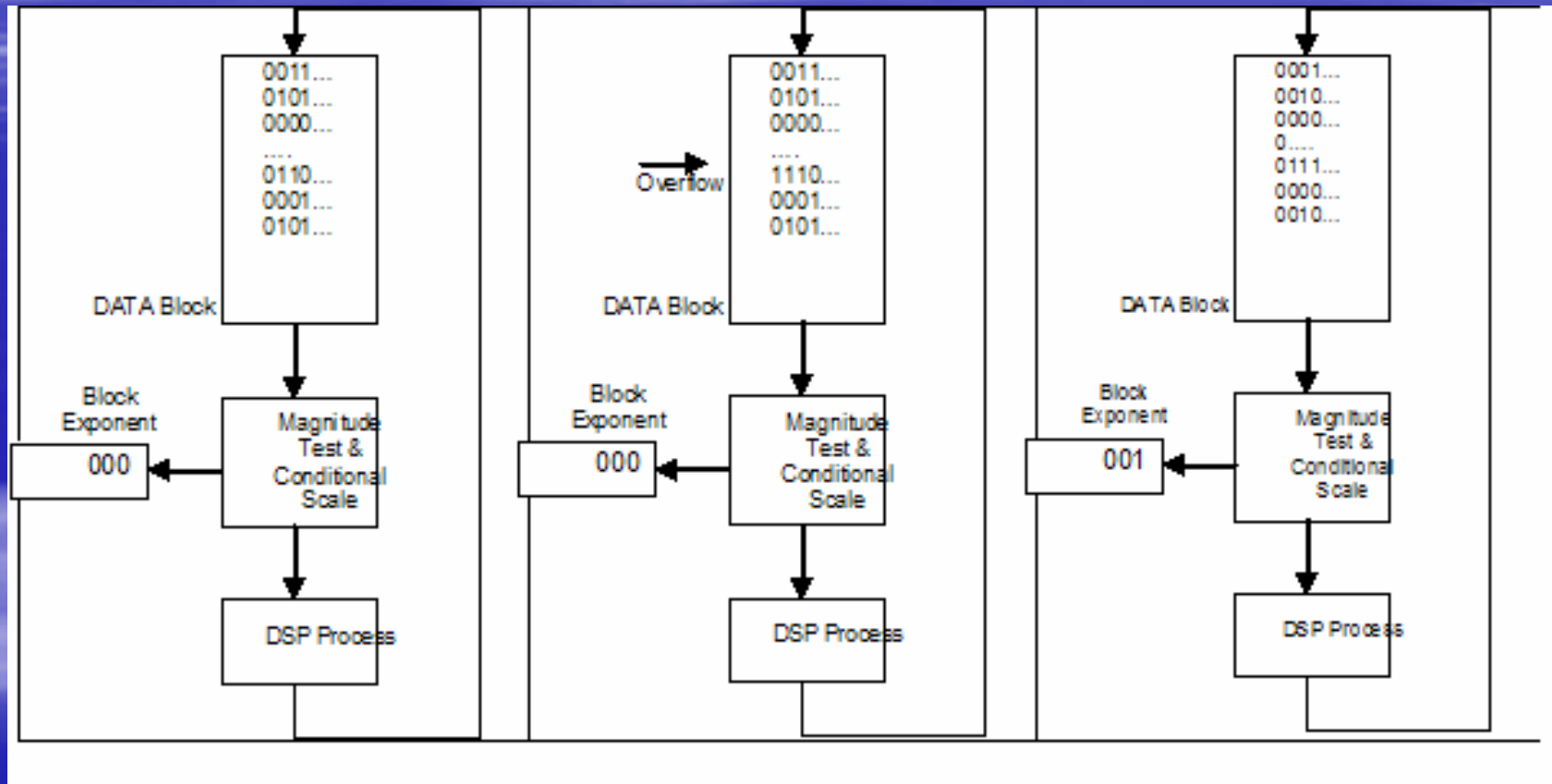
Outline

- BFP Arithmetic
 - Why BFP?
- Our Case Study
 - Error Analysis
- Solutions
- Simulation Results
- Conclusion
- References

BFP Arithmetic

- Floating-Point or Fixed-Point Realizations
- Block Floating Point
- This structure first delivered by A. V. Oppenheim

BFP Arithmetic



Why BFP?

- Very bit effective
- Exactness close to floating-point (FP) arithmetic
- Implementable with fixed-point DSPs
- In many structures, considering the smallest HW (for fixed point structures) will cause a large error. Otherwise, the HW will grow very large.
- For example, in our FPGA time/equalizer example with 16 taps, the number of overflows is around 2.26 in calculation of each output [7]. Considering the worst case, we should add 4 more bits for 16 additions.
- Floating Point is very complicated.
- Block-floating-point method is a compromise between these two methods.

Why BFP?

- BFP arithmetic has been used in different kinds of signal processing applications, such as recursive digital filters [4]-[6] .
- We note that BFP structure is defined as the number representation algorithm in several digital audio data transmission standards such as NICAM (stereo-phonic sound system for PAL TV standard) [13], the audio part of MUSE (Japanese HDTV standard) [14], and DSR (German Digital Satellite Radio system) [15].

Our Case Study

- It is widely accepted that the quantization error contained by using rounding function is less than the quantization error with truncation [11].
- However, in systems using BFP, there are cases where the rounding error becomes larger than the truncation error.
- This happens, for example, with numbers which have a LSB of one and their other bits are zeros, and for occurrence of more than one consecutive rounding operation
- This Issue First observed when we where implementing a Time equalizer of an ADSL modem

Error analysis?

- This problem occurs when in the calculation of one system output, more than one overflow occurs in a block of data.
- The main problem is the possible propagation of "one" from the LSB to the more significant bits.

Example

- Consider 00100001 with power=0; after first time of shifting and rounding.
- It will become 0010001 and power=1, after second time of shifting and rounding.
- It will become 001001 and power=2, which is equal to $001001 * 2^2 = 00100100$.
- After 2 times of shifting and truncation, it will become 001000 with power=2, which is equal $001000 * 2^2 = 00100000$ which is closer to the original value 00100001.

Solutions

- Using a new rounding function which prevents such propagations by rounding the odd "ones" and truncating the even "ones" when they are spared.
 - For example, consider the number 00100001 with power=0. After the first shift and rounding, it will become 0010001 with power=1, after the second time of shift and truncation, it will become 001000 with power=2, which is equal to $001000 \cdot 2^2 = 00100000$ that is now closer to 00100001.

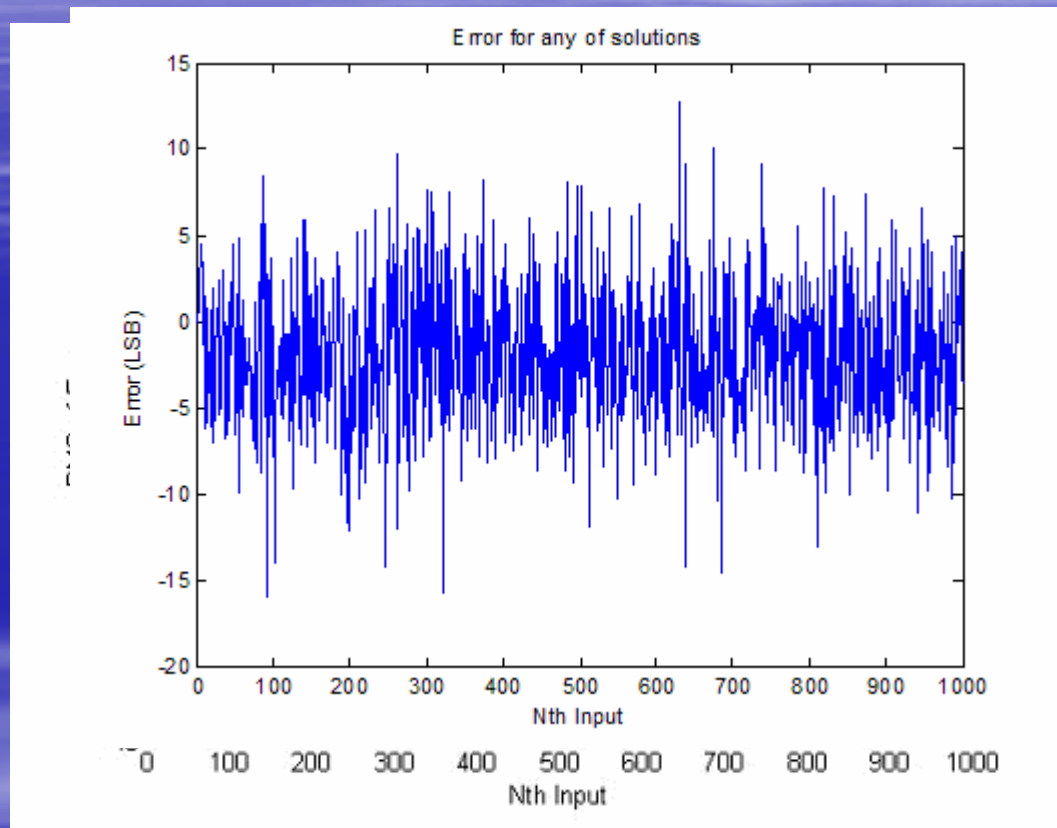
Solutions

- Using a barrel shifter before the accumulator and shifting the input numbers by the overall number of overflows which has already occurred and then rounding the input
 - This method is more effective for FIR filters since after their forward operations, it is not necessary to return the output values back in the block.

Simulation results

- Case one; Coefficients set to highest level (for maximizing the number of over flow):
 - Using rounding, the RMS of the error is $1328.4 * \text{LSB}$; using truncation it became $1332 * \text{LSB}$; using one of the solutions made the error equal to $472.77 * \text{LSB}$.
- Case two; Coefficients set with chow algorithm:
 - Using rounding, the RMS of error was $349 * \text{LSB}$; using truncation made the error $595.68 * \text{LSB}$; using any of our solutions made it equal to $152.79 * \text{LSB}$.

Simulation results



Error when using the proposed solutions
Truncating error

Conclusion

- We reported one degrading issue observed when using block-floating-point arithmetic in the time equalizer of an ADSL modem.
- Neglecting this issue may increase the round-off error significantly and reduce the SNR of some systems.
- Fixing this issue may reduce RMS of errors by a factor of 2 in this time equalizer which equalizes the CSA6 channel of an ADSL modem.
- we described two solutions to remedy this problem.

References

- J. Konro et al., "Floating-point arithmetic in signal processing," in *proc. 1992 IEEE International Symposium on Circuits and Systems*, San Diego, CA, USA, May 10-13, 1992, pp.1784-1791.
- K. Kalliojärvi et al., "Roundoff errors in block-floating-point systems," *IEEE Trans. Signal Processing*; vol. 44, no. 4, April 1996.
- Arun Chhabra, Ramesh Iyer "A Block Floating Point Implementation on the TMS320C54x DSP.", Application Report, SPRA610 - December 1999, retrieved from: <http://focus.ti.com/docs/apps/catalog/resources/appnoteabstract.ihtml?abstractName=spra610>, on 2004-11-12.
- Alan V. Oppenheim, "Realization of digital filters using block-floating-point arithmetic," *IEEE Transactions on Audio and Electroacoustics*, vol. AW-18, no. 2, June 1970.
- D. Williamson et al., "A new approach to block floating point arithmetic in recursive digital filters," *IEEE Trans. Circuits Syst.*, vol. CAS-32, no. 7, pp.719-722, July 1985.
- S. Sridharan and D. Williamson, "Implementation of high-order direct-form digital filter structures," *IEEE Trans. Circuits Syst.*, vol. CAS-33, no. 8, pp. 818-822, Aug. 1986.
- A. V. Oppenheim and C. J. Weinstein, "Effects of finite register length in digital filtering and the fast Fourier transform," in *proc. IEEE*, vol. 60, no. 8, pp. 975-976, Aug. 1972

References

- A. C. Erickson and B. S. Fagin, "Calculation the FHT in hardware," *IEEE Trans. Signal Processing*, vol. 40, no. 6, pp. 1341-1353, June 1992.
- American National Standard for Telecommunications, Network and Customer Installation Interfaces, Asymmetric Digital Subscriber Line (ADSL) Metallic Interface. ANSI Standard T1.413-1998, 1998.
- H. Mahdiani, "Optimization and Hardware Modeling of the DMT Engine of an ADSL Modem for ASIC Implementation," M. Sc. thesis, Electrical and Computer Engineering Department, University of Tehran, 2001.
- Lars Wanhammar, "DSP Integrated Circuits" published by Academic Press, 2001.
- J. S. Chow, J. M. Cioffi, J. A. C. Bingham, "Equalizer training algorithms for multicarrier modulation system", *IEEE Int. Conf. Commun.*, vol. 1, pp. 761-765, 1993.
- A. J. Bower, "Digital two-channel sound for terrestrial television," *IEEE Trans. Consum. Electron.*, vol. CE-33, no. 3, pp. 286-296, Aug. 1987.
- Y. Ninomiya et al., "An HDTV broadcasting system utilizing a bandwidth compression technique – MUSE," *IEEE Trans. Broadcasting*, vol. BC-33, no. 4, pp. 130-160, Dec.1978.
- O. klank and D. Rottmann, "DSR-receiver for the digital sound broadcasting via the European satellites TV-SAT/TDF," *IEEE Trans. Consum. Electron.*, vol.35, no. 3, pp. 504-511, Aug. 1989.

Thank You for Your Attention