Implementation of a High-Speed Low-Power 32-bit Adder in 70nm Technology

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Outline

- Introduction
- Comparing two 4-bit adders in different logics
- Introducing a proper sense amplifier
- 32-bit adder implementation
- Conclusion
Introduction

- Technology has stepped towards Deep Sub Micron (DSM) dimensions.
- What is the best DSM technique of logic-circuit implementation to have the highest speed and the lowest power dissipation?
- Low Voltage Swing (LVS) technique has been considered as an efficient way to reduce power consumption while reaching higher speeds.
One Stage of a 4-Bit Adder in Fully Differential Dual-Rail Domino Logic

Sum Generator [9]

Carry Generator [9]
The Adder is implemented in 70nm technology with 0.9V voltage supply.

Maximum of 3GHz clock can be reached for this circuit.
How to Get Higher Speeds?

- LVS (Low Voltage Swing) technique can be used to improve the performance of some circuits.

- Applying this technique in DCN (Diffusion Connected Network) pass transistors in critical paths of a circuit will evaluate the logic functions which have low voltage swing.

- The output voltage swing of this kind of structure finds standard voltage swing using sense amplifiers.
One stage of a 4-bit LVS adder [modified version of the same figure in [7])

- P, G, and K are Propagate, Generate, and Kill signals respectively, that can be implemented by CDL or static logics.
- All drains are predischarged in the reset phase.
- Level 1 of the clock is the evaluation phase of the circuit.
- Signals propagate through the chain differentially.
A simulation of the LVS adder was performed using 70nm technology with 0.9V power supply.

Maximum of 10GHz clock frequency can be reached for this circuit.

Outputs have low voltage swings, therefore, they need sense amplifiers to reach the standard voltage level.
Two sense amplifiers were found that could possibly be used in LVS circuits.

Latched Sense Amplifier (LSA) [7]
Sense Amplifiers (2)

Sense Amplifier with Flip-Flop (SAFF) [10]
## Comparison between SAs

<table>
<thead>
<tr>
<th></th>
<th>SAFF</th>
<th>LSA</th>
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<tbody>
<tr>
<td>Technology</td>
<td>70nm</td>
<td>70nm</td>
</tr>
<tr>
<td>Max freq</td>
<td>4GHz</td>
<td>10GHz</td>
</tr>
<tr>
<td>Minimum Amplifiable Input Level</td>
<td>0.3V</td>
<td>0.1V</td>
</tr>
</tbody>
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Therefore, LSA is more proper for our design.
16 blocks of the single-stage LVS adder are cascaded. A carry-skip network is used so the signals do not have to pass through more than 6 transistors. Si’s are controlled with propagate signals.

Carry Skip Network [7]
Output Waveform

16-bit carry-skip adder output waveform in 70nm technology after passing though the SAs
New 32-Bit Carry-Select Adder

A[0..15] B[0..15]

CI

16-bit adder

CO15

SUM[0..15]


CI

16-bit adder

CO15


CI

16-bit adder

CO15

s

MUX2-1

CO31

SUM[16..31]
## Comparison Table

<table>
<thead>
<tr>
<th></th>
<th>16 bit adder</th>
<th>32 bit adder</th>
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<tbody>
<tr>
<td>Max freq</td>
<td>10GHz</td>
<td>10GHz</td>
</tr>
<tr>
<td>Max ( t_p )</td>
<td>97 ps</td>
<td>99 ps</td>
</tr>
<tr>
<td>avgpower</td>
<td>0.97 mW/GHz</td>
<td>2.58 mW/GHz</td>
</tr>
<tr>
<td>maxpower</td>
<td>2.93 mW/GHz</td>
<td>7.71 mW/GHz</td>
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Conclusion

- LVS appears as a proper technique in designing high-speed low-power logic gates in DSM technologies.
- With this technique, a 32-bit adder can be implemented in 70nm technology with 10GHz clock frequency and power dissipation of as low as 2.58 mW/GHz.
Thank You

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