

# Curriculum Vitae

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## Personal Information:

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First Name : Mahdi  
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University of Tehran, 16<sup>th</sup> Street, North Kargar Avenue  
Tehran, IRAN.

## Education:

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- **2003 – 2006:** M. Sc., Computer Architecture, University of Tehran, Tehran (GPA = 18.03/20)  
***M. Sc. Thesis Title:*** Design and Implementation of Efficient Algorithms for Video Coding (Grade = 20/20)  
***Supervisor:*** Prof. S. Omid Fatemi, email: [omid@fatemi.net](mailto:omid@fatemi.net)  
***Advisor:*** Prof. Mahmud Reza Hashemi, email: [hashemi@comnete.com](mailto:hashemi@comnete.com)
- **1999 – 2003:** B. Sc., Computer Architecture, University of Shiraz, Shiraz (GPA = 16.48/20)  
***B. Sc. Project Title:*** Modeling and Simulation of Data Communications Methods using VHDL Language.
- **1998 – 1999:** Diploma, Mathematics and physics, Shahid Beheshti High School, Bojnord (GPA = 19.48/20)

## Awards:

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**1999 – 2003:** Rank 1<sup>st</sup> between both hardware and software graduated students in Computer Science and Engineering Department, University of Shiraz.

## Research Interests:

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- **Multimedia System:** Video Compression, Audio Compression, Audio/Video over IP.
- **High-Performance Architecture Design:** Multi-level parallel architectures, Stream Processors.
- **Embedded Systems:** Embedded Processors, HW/SW Co-Design
- **Network on Chip:** Communication Schemes, Protocols Design.
- **Design, Verification and Test:** NoC Testing, Core Testing, Online testing, Self-testing, Memory testing.
- **Design of Security Systems:** Video/Audio Encryption, Watermarking, IPsec

## Technical Skills:

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- **Programming:**  
Verilog, VHDL, C/C++, DirectShow, Java, C#, ASP web programming, Assembly language, C--, Rexx, SmallTalk, Python.
- **Tools:**  
Microsoft Visual Studio, Synopsys tools (Design Compiler, PrimePower, TetraMax ATPG, Formality, HSPICE), Xilinx Development tools (XPS, ISE), Leonardo Spectrum, ModelSim, NCSim, Active HDL, Protel PCB Designer, Quest3D game engine.

## Research Experience:

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- **2009–now: Researcher, SINA Microelectronics Co., Tehran, Iran**
  - Ad-hoc and mobile mesh network protocols
  - Mobile multimedia application design
- **2007–2009: Researcher, NAJI Research and Development Co., Tehran, Iran**
  - HW/SW development of a 3D Car Driving Simulator (AMER)
  - Implementing data management in AMER system
- **2006–2008: Research Assistant, Silicon Intelligence and Advanced VLSI Signal Processing Lab., School of ECE, University of Tehran, Iran**
  - Designing and implementation of a simulator for VLIW DSPs
  - Design and development of a multi-DSP architecture (MDST)

- **2004 – 2006: Research Assistant, Multimedia Processing Lab., School of ECE, University of Tehran, Iran**
  - Designing Hardware Accelerator for H.264/AVC VBSME
  - Optimizing the Mode Decision Algorithm for H.264/AVC
  - Designing Hardware Accelerator for H.264/AVC Deblocking Filter
  - Designing 2-D Deblocking Filter for H.264/AVC
  
- **2003–2004: Research Assistant, Silicon Intelligence and Advanced VLSI Signal Processing Lab., School of ECE, University of Tehran, Iran**
  - Designing a MIPS like embedded processor for Education
  - Developing an Assembler for the proposed MIPS like Processor
  
- **2002–2003: Research Assistant, Network Lab., Department of CSE, University of Shiraz, Iran**
  - Modeling and Simulation of Data Communications Methods using VHDL Language

## **Teaching Experience:**

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- **Fall 2009:** Computer Engineering Dept., Qazvin Islamic Azad University, Qazvin, Iran
  - Fundamentals of Computers
  - Advanced Programming
  - Computer Architectures
  
- **Spring/Fall 2009:** Computer Engineering Dept., School of Virtual University at Shiraz University, Tehran.
  - Data Structures
  - Assembly and Machine Languages
  - Scientific and Technical Presentation
  
- **Fall 2008:** Computer Engineering Dept., Elmi-Karbordi University, Tehran.
  - Computer Architectures
  - Microprocessors
  
- **2007–2008:** Computer Engineering Dept., International Branch, Shiraz University, Shiraz.
  - Data Structures
  - Data Communications
  - Design of Compilers
  - Theory of Machines and Languages
  - Object Oriented Programming (JAVA)
  - Design and Implementation of the programming languages
  - Advanced Programming (C)

## Work Experience:

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- **2009 – Now: System Design Engineer, Secure Mobile Mesh Network, SINA Microelectronics, Tehran, Iran**
  - Multimedia communication
  - Ad-hoc Mesh network protocol
- **2007 – 2009: Design Engineer, NAJI Research and Development Co., Tehran, Iran**
  - Board level design of data acquisition and sensors for AMER simulator
  - Controlling and Auto-Instruction system of AMER
  - Design of record and network management system for AMER
  - Implementation of the physical parts of AMER in the 3D simulation environment
- **2004 – 2007: Design and Verification Engineer, Internet Broadband Gateway (IBG), SiNA Semi. Co, Tehran, Iran**
  - Verification of the IBG
  - Design and Verification of the IPSec and MBIST block
  - Verification of the UTOPIA block
- **2003: Design Engineer, ITMC Co., Shiraz, Iran**
  - ISA Expansion Card for Monitoring V.5 Signaling Protocols

## Teaching Assistantships:

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- **2004:** Advanced VLSI Design, School of Electrical and Computer Engineering, University of Tehran.
- **2001:** Logic Circuits, Computer Science and Engineering Department, University of Shiraz.

## Publications:

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### *Journal Papers*

1. N.Sedaghati-Mokhtari, **M.N. Bojnordi**, A. Hormati, S.M. Fakhraie, "VLIW DSP Processors: An Efficient and Extendable Modeling Approach," submitted for publication.
2. N. Sedaghati-Mokhtari, **M. Nazm-Bojnordi**, A. Hormati, and S. M. Fakhraie, "Efficient Modeling of VLIW DSP Processors," *Communications in Computer and Information Science (CCIS 6)*, pp. 267–274, 2008.
3. **M.N. Bojnordi**, N. Sedaghati-Mokhtari, "STAR: an efficient self transposing architecture for 32-bit data processors," *Iranian Journal of Engineering Sciences (IJES)*, vol. 1, no. 1, 2008.

## Conference Papers

1. **M.N. Bojnordi**, O. Fatemi, M.R. Hashemi, "An efficient deblocking filter with self-transposing memory architecture for H.264/AVC," *IEEE International Conference on Acoustics, Speech, and Signal Processing (ICASSP)*, vol. 2, pp. 925–928, France, May 2006.
2. M. Hosseinabady, A. Banaiyan, **M.N. Bojnordi**, Z. Navabi, "A concurrent testing method for NoC switches," *Design, Automation, and Test in Europe Conference (DATE)*, Germany, March 2006.
3. N. Sedaghati–Mokhtari, **M. N. Bojnordi**, S. M. Fakhraie, "MDST: Multiprocessor DSP Simulation Toolkit for Voice Processing Applications," *IEEE / ACM International Symposium on Modeling, Analysis, and Simulation of Computer and Telecommunication Systems (MASCOTS)*, pp. 173–179, Turkey, October 2007.
4. **M.N. Bojnordi**, M.R. Hashemi, O. Fatemi, "A fast two dimensional deblocking filter for H.264/AVC video coding," *Canadian Conference on Electrical and Computer Engineering (CCECE)*, June 2006.
5. **M.N. Bojnordi**, O. Fatemi, M.R. Hashemi, "Dual mode architecture for deblocking filtering in H.264/AVC video coding," *IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*, pp. 1770–1773, Singapore, December 2006.
6. **M.N. Bojnordi**, O. Fatemi, M. Semsarzadeh, M.R. Hashemi, "Efficient hardware implementation for H.264/AVC motion estimation," *IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*, pp. 1774–1777, Singapore, December 2006.
7. **M.N. Bojnordi**, M.R. Hashemi, and S.O. Fatemi, "Implementing an efficient encryption block for MPEG video streams," *IEEE International Symposium ELMAR*, pp. 127–130, Croatia, June 2005.
8. **M.N. Bojnordi**, N. Moezzi–Madani, M. Semsarzadeh, A. Afzali–Kusha, "An efficient clocking scheme for on–chip communications," *IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*, pp. 119–122, Singapore, December 2006.
9. **M.N. Bojnordi**, N. Sedaghati–Mokhtari, O. Fatemi, M.R. Hashemi, "An efficient self-transposing memory structure for 32–bit video processors," *IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*, pp. 1484–1487, Singapore, December 2006.
10. M. Hosseinabady, **M.N. Bojnordi**, A. Banaiyan, Z. Navabi, "An efficient online BIST architecture for NoCs," *European Test Symposium (ETS)*, London, UK, pp. 97–102, 2006.
11. **M. Nazm–Bojnordi**, M. Semsarzadeh, A. Banaiyan, A. Afzali–Kusha, "A simple, low–cost and low–power switch architecture for NoCs," *IEEE International Conference on Microelectronics (ICM)*, pp. 194–197, Pakistan, 2005.
12. N. Sedaghati, **M. N. Bojnordi**, and N. Yazdani, "Cross–layer design: a new paradigm," *International Symposium on Communication and Information Technology (ISCIT)*, no. w3c–4, Thailand, October 2006.

13. **M. Nazm-Bojnordi**, N. Sedaghati-Mokhtari, S. M. Fakhraie, "A self-testing fully pipelined implementation for the advanced encryption standard," *IEEE International Conference on Microelectronics (ICM)*, pp. 260–263, Pakistan, 2005.
14. N. Sedaghati-Mokhtari, **M. N. Bojnordi**, A. Farmahini-Farahani, M. Mousavinezhad, and S. M. Fakhraie, "Simulation of voice processing applications through VLIW DSP architectures," *IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, pp. 291–293, Morocco, December 2007.
15. **M.N. Bojnordi**, O. Fatemi, M. Semsarzadeh, M.R. Hashemi, "Block Merging Motion Estimation for Fast Mode Decision in H.264/AVC Video Coding," *GSPx, TV to Mobile*, Netherland, March 2006.
16. N. Sedaghati-Mokhtari, **M. N. Bojnordi**, S. M. Fakhraie, "An Efficient and Extendable Modeling Approach for VLIW DSP Processors," *Computer Society of Iran Computer Conference (CSICC)*, Iran, March 2008.

## References:

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Prof. F. Sobhanmanesh, Shiraz University, email: [fsobhanmanesh@yahoo.com](mailto:fsobhanmanesh@yahoo.com)  
Prof. S. Omid Fatemi, University of Tehran, email: [omid@fatemi.net](mailto:omid@fatemi.net)  
Prof. M. R. Hashemi, University of Tehran, email: [hashemi@comnete.com](mailto:hashemi@comnete.com)  
Prof. Sied Mehdi Fakhraie, University of Tehran, email: [fakhraie@ut.ac.ir](mailto:fakhraie@ut.ac.ir)  
Prof. Zeinalabedin Navabi, University of Tehran, email: [navabi@ece.neu.edu](mailto:navabi@ece.neu.edu)  
Prof. Ali Afzali Kusha, University of Tehran, email: [afzali@ut.ac.ir](mailto:afzali@ut.ac.ir)  
Mr. F. Baharvand, SiNA Semi Co., email: [fbahrvand@sinamicro.com](mailto:fbahrvand@sinamicro.com)