A Concurrent Testing Method for NoC Switches

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Abstract

This paper proposes reuse of on-chip networks for testing switches in Network on Chips (NoCs). The proposed algorithm broadcasts test vectors of switches through the on-chip networks and detects faults by comparing output responses of switches with each other. This algorithm alleviates the need for: (1) external comparison of the output response of the circuit-under-test with the response of a fault free circuit stored on a tester (2) on-chip signature analysis (3) a dedicated test-bus to reach test vectors and collect their responses. Experimental results on a few test benches compare the proposed algorithm with traditional System on Chip (SoC) test methods.

1. Introduction

RECENT advances in IC design methods and manufacturing technologies allow designers to integrate the complete system on a single chip. This so-called SoC product class is a yet-evolving design style that integrates technology and design elements from other system driver classes into a wide range of high-complexity, high-value semiconductor products [1]. Even though commercial products currently exhibit only a few integrated cores [2], in the next few years, technology will allow the integration of thousands of cores, making a large computational power available.

Today's System on Chip (SoC) technology can achieve unprecedented computing speed that is shifting the IC design bottleneck from computation capacity to communication bandwidth and flexibility[3]. Also, since communication buses between the cores are not sufficiently scalable, bus-based SoCs (the common type of SoCs) cannot handle this high volume of communication between the cores in the SoCs. In addition, these SoCs cannot be used for high speed serial communications. Moreover, as volume of the data communication on the chip increases, the power consumption increases. Therefore, a scalable communication infrastructure that better supports the trend of state-of-the-art SoC integrations is required. Thus, recent researchers use packet-switched micro-network on a chip, so called NoC, as a scalable communication media. The basic idea is borrowed from traditional large-scale multi-processors and the wide-area network domains.

It is important that SoC designers consider a test methodology for their new SoC architectures. Like other SoCs, an NoC has to be tested for manufacturing defects. One of the main problems for testing an SoC is the access to the cores during the test process [4]. A number of solutions have been presented in the literature [5] [6] to solve this problem while minimizing test costs, mainly pin count and test time. Most methods rely on scalable and easy-to-design test access mechanisms (TAMs) to reduce design time. For those methods, bus-based TAMs are usually chosen. Since the NoCs consist of functional cores, switch cores and interfaces, test methodologies should be performed on each of these three parts.

This paper proposes a novel concurrent test methodology for testing the switches of an NoC. The rest of the paper is organized as follows. Related works on testing the SoC and NoC are reviewed in Section 2. Section 3 introduces some preliminaries and definitions. Our proposed algorithm is discussed in Section 4. In our proposed algorithm, a wrapper architecture is proposed for the switches and this is discussed in Section 5. In Section 6 test time calculation will be described. The proposed switch architecture will be discussed in Section 7. Finally the paper ends with experimental results and conclusions.

2. Related Works

A packet switching communication-based TAM for an SoC has been proposed in [7]. The proposed TAM model is called NIMA, and it is defined for the test task. Thus, routing and addressing strategies are defined considering only the test requirements of each system. Test and verification challenges for system chips that utilize on-chip network has been presented in [8]. In [8] an NoC has been exemplified by Philips' ÆTHEREAL NoC architecture. It shows the particular advantages of using an NoC for both testing and verifying the network components, and testing and verifying the other components of the SoC. The reuse of functional connections during test has been suggested in the literature [9][10]-[13] to reduce test costs in terms of area and pin overhead. For those methods, a core-to-core connection model is assumed. The impact of the reuse of an on-chip network for the test of core-based systems is described in [14], [15]. These references formalize a reuse strategy aiming at minimizing the system test costs. A network-based embedded core testing architecture using

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