

An Efficient Online BIST Architecture for NoCs

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Abstract

This paper presents an offline/online concurrent scan based built-in-self-test (scan-BIST) method for a Network-on-Chip (NoC) based SoC. The proposed architecture contains a special scan cell and an Embedded Test Core (ETC) as its test source. The ETC performs a static flow control and a centric average power consumption control during the proposed test mechanism. To reduce the test vector traffic, the ETC uses a multicasting approach to send a test vector to multiple cores, simultaneously. Inserting only one clock cycle stall in the normal operation of a core, the proposed cell architecture applies a test vector to the core-under-test and captures its output response.

1. Introduction

Very deep-submicron technologies pose new challenges to IC testing. In particular, in the system-on-a-chip (SoC) design, crosstalk and transient faults are difficult to detect with traditional methods. Transient faults may cause a failure of a circuit where only data are lost (e.g., a bit-flip) or may cause a damage in the internal structure of the semiconductor material that results in a permanent fault. The former form of transient faults is called *soft-errors* and the latter is called *hard-errors*. Online testing technique is one of the approaches that can detect hard-errors.

The increasing use of portable computing and wireless communication and also the growing transistor density and the increasing operation frequency in very large scale integrated circuit have made power dissipation an important issue in both design and test. Power dissipation during testing the circuit should be considered by the designers.

In some of the previous works on SoC testing, test stimuli and test results are transported through a Test Access Mechanism (TAM) [1]. In most of these approaches a bus is used for TAM. In these methods the bus and a few controlling signals are arranged to send test vectors directly to the core-under-test. The new SoC design methodologies focus on communication rather than the computation [2]. These methodologies use a network-on-chip (NoC) as the communication media among cores of the SoC. As it becomes impossible to move signals across a large die within one clock cycle or in a power-effective manner, or to run control and dataflow processes at the same clock rate, the likely result is a shift to asynchronous or globally asynchronous and locally synchronous (GALS) design style. So in these SoCs, using the bus to create a bridge among source and sink of test data and the core-under-test is impossible, proposing a test method based on the GALS mechanisms is necessary. In [3] some test architectures are

proposed considering the requirements for transferring test data among test source, test sink and the cores, through existing interconnects of the SoC. These test architecture are more adapted with an offline and off-chip test mechanisms.

This paper proposes an *online/offline concurrent test* architecture for the *logic cores* in an NoC based SoCs which addresses the following issues: communication centric structure of the NoC, test power, and performance degradation during online testing. The proposed approach is a scan-BIST architecture using an online test mechanism for communication centric SoCs in which the test patterns are distributed through the NoC from a test source. For this purpose, the proposed architecture defines one or more test sources, called **Embedded Test Cores** (ETC), to distribute test patterns for cores inside the SoC. The test patterns are transmitted to the cores in the form of test packets through the NoC. To reduce the traffic caused by the test mechanism in the switches, each core has its own output response analyzer (ORA) to generate the signature of captured responses. For more reduction in overloaded test traffic, ETC multicasts a test packet through the NoC to test more than one core at any given time. Furthermore, we propose a scan cell architecture for cores that gets the test pattern during the normal operation of the cores and applies it to the core in one clock cycle. Therefore, this architecture inserts just one clock stall for applying each test vector to the core during its normal operation. Using a simple control mechanism, ETC controls the average test power dissipation in the cores.

The rest of the paper is organized as follows. The next section describes our test methodology where our main contributions are discussed. Section 3 describes the test architecture in cores that includes our proposed scan cell architecture, and signature analyzer. Section 4 explains the different parts of the ETC and their architectures. This section also contains the traffic and power reduction techniques. The architecture and protocols of network layer are described in Section 5. Experimental results are demonstrated in Section 6. Finally, Section 7 concludes the paper and points to the future work.

2. Test Methodology

In an NoC based SoC, a network of switches tackles the burden of the communication among the cores. The network of switches may have heterogeneous or homogeneous topologies. Some examples of homogeneous NoC topologies include grid, tours, hypercube, ring, multi-stage, and fat-tree.

To implement an online test mechanism in an SoC, several issues should be considered: