

AN EFFICIENT DEBLOCKING FILTER WITH SELF-TRANSPOSING MEMORY ARCHITECTURE FOR H.264/AVC

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ABSTRACT

One of the main reasons behind the superior efficiency of the H.264/AVC video coding standard is the use of an in-loop deblocking filter. Since the deblocking filter is computation and data intensive, it has a profound impact on the speed degradation of both encoding and decoding processes. In this paper, we propose an efficient deblocking filter architecture that can be used as an IP core either in the dedicated or platform-based H.264/AVC codec systems. Novel self-transposing memory unit is used in this paper to alleviate switching between the horizontal and vertical filtering modes. Moreover, to reduce the processing latency, a two-stage pipelined architecture is designed for 1-D filter that produces output data after 2 clock cycles. With a clock of 100 MHz the proposed design is able to process a 1280×1024 (4:2:0) video at 25 frame/second. The proposed architecture offers 33% to 56% performance improvement compared to the existing state-of-the-art architectures.

1. INTRODUCTION

Most video coding techniques employ block-based prediction, transformation, and quantization for encoding. The use of these block-based tools, however, decreases inter-block correlation in video frames and adds visible blocking structures to the reconstructed frame, i.e. blocking artifacts [1]-[3]. The newest video coding standard, H.264/AVC [4], uses an in-loop adaptive filter to eliminate the blocking artifacts. Among various coding tools of the H.264/AVC codec, the in-loop deblocking filtering module has a profound impact on the video visual quality improvement [5]. However this improvement is achieved at the cost of large amount of computation and memory read/write operations. Therefore its computational complexity significantly reduces the encoding/decoding speed. The deblocking filter is described in detail in [6]. The advantages of the in-loop deblocking over post filters are also discussed in this reference. As shown in [1], the in-loop deblocking filter reduces the bit-rate typically by 5%-10% preserving the same objective video quality.

Recently, there are many proposed architectures for H.264/AVC deblocking filter [7]-[11]. Generally, in order to design an efficient real-time architecture for H.264/AVC deblocking filter, two major issues should be addressed, including 1-D filter processing latency and memory data access.

In this paper, a high-performance low-cost deblocking algorithm is proposed. Using an efficient memory management and self-transposing memory architecture, performance improvement of up to 56% is achieved, compared to the existing state-of-the-art architectures. The paper is organized as follows. An introduction to the H.264/AVC deblocking algorithm is given in Section 2. In Section 3, our proposed architecture is described. Comparison and experimental results are presented in Section 4. Finally, the paper ends with a conclusion Section 5.

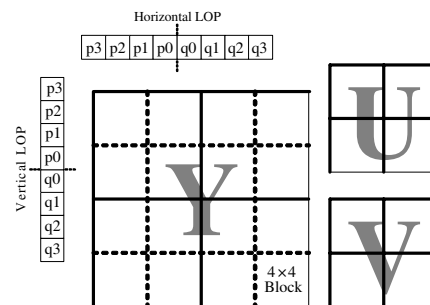


Fig. 1- Macroblock boundaries that should be filtered in each of the three Y, U, and V components.

2. THE H.264/AVC DEBLOCKING ALGORITHM

According to the latest H.264/AVC Recommendation [4], the deblocking filtering algorithm is defined as a conditional process that has to be applied to vertical and horizontal edges of all $N \times N$ blocks of each macroblock. For luminance component (Y) N is selected equal to the size of the applied I-transform, i.e. 4 or 8. For chrominance components (U and V) N is selected equal to 4. Fig. 1 shows the boundaries inside a macroblock that have to be filtered. The boundaries indicated by bold lines should be filtered for both sizes of applied transform. However, the edges indicated by dotted