Data-Driven Dynamic Logic versus NP-CMOS Logic, A Comparison

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ABSTRACT

Data-Driven Dynamic Logic (D\textsuperscript{3}L) is an appropriate candidate for replacing conventional dynamic logic in many cases. In our previous paper, we have shown how a D\textsuperscript{3}L-based design can be used in place of a conventional Domino logic [1]. The designed circuit has been shown to have up to 30\% less power dissipation compared to its Domino counterpart. This is in addition to the fact that no speed degradation was found. In this paper, after a brief introduction on NP-CMOS logic and D\textsuperscript{3}L, we show how to convert an NP-CMOS design to a D\textsuperscript{3}L one. Then the results of simulations performed on a 16-bit barrel shifter are demonstrated and compared for static, NP-CMOS and D\textsuperscript{3}L design styles.

1. INTRODUCTION

Historically, complementary logic came after NMOS and pseudo-NMOS styles to overcome static power consumption of NMOS logic family. However, CMOS logic comes with an area overhead, as a specific logic must be complementarily duplicated in both of a pull-up network (PUN) and a pull-down network (PDN). Improvements of CMOS technology and reduction of minimum feature sizes compensated part of this area overhead. However, one should note that logic duplication in CMOS has an effect on increased node capacitances, beside extra power consumption, that could not be ignored.

A major challenge is looking for solutions by which to avoid logic duplication in CMOS without static power consumption of NMOS logic family. Dynamic logic style provides an answer for this question [2]. In dynamic logic, logic function appears in only one of PUN or PDN branches, and a global clock signal provides the functionality of PUN or PDN branch. Thus, the circuit operation is divided in two distinct precharge and evaluate phases. In the precharge phase, charge is pumped from V\textsubscript{DD} to the output node (\textit{M\textsubscript{p}} in Fig. 1), while \textit{M\textsubscript{e}} is turned off and the current path to ground is disconnected [2].

Compared to CMOS, dynamic logic can improve speed and reduce area. However, But these benefits do not come for free. Presence of a foot transistor increases logic evaluation time, the clock signal must drive every dynamic logic gates in addition to registers, and it will be faced with heavy loads. Besides this, it oscillates permanently resulting in high activity factor and considerable power consumption [3]. Moreover, for correct evaluation of dynamic gates, a set of conditions must be imposed on the inputs of every dynamic block. For example, in the Domino logic style [2], a static inverter follows every \textit{Φ-N} block. This ensures that all inputs to the next logic block are set low after the precharge period. This means that it might be difficult to implement some functions and the designers must take additional procedures.

We summarize the advantages of dynamic logic styles compared to CMOS logic in two main categories. The first one is speed improvement and the second is area reduction. Its disadvantages are higher power consumption, especially on clock signal, presence of the foot transistor (Fig. 1) that adds some delay and power consumption, and a more difficult design process. We show that D\textsuperscript{3}L improves conventional dynamic logic functionality and reduces its disadvantages, namely, relaxes its excessive power consumption. Some details come in the next section.

2. DATA-DRIVEN DYNAMIC LOGIC

In this section, we describe D\textsuperscript{3}L design concept. In creation of conventional dynamic logic, a set of conditions is imposed on dynamic blocks. These conditions are arranged such that the logic transistors stay in \textit{off} state during the precharge time. This condition is necessary for correct operation at the beginning of the evaluation phase and prohibits the output node from accidental discharge. In D\textsuperscript{3}L, we use these existing conditions to find a replacement for the clock signal.

For example, consider a 2-input \textit{AND} gate in Domino logic, implemented as shown in Fig. 1. As noted in this figure, both of the inputs \textit{A} and \textit{B} are held at a low level in the precharge phase. The circuit operation is divided in two distinct precharge and evaluate phases. In the precharge phase, charge is pumped from V\textsubscript{DD} to the output node (\textit{M\textsubscript{p}} in Fig. 1), while \textit{M\textsubscript{e}} is turned off and the current path to ground is disconnected [2].

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